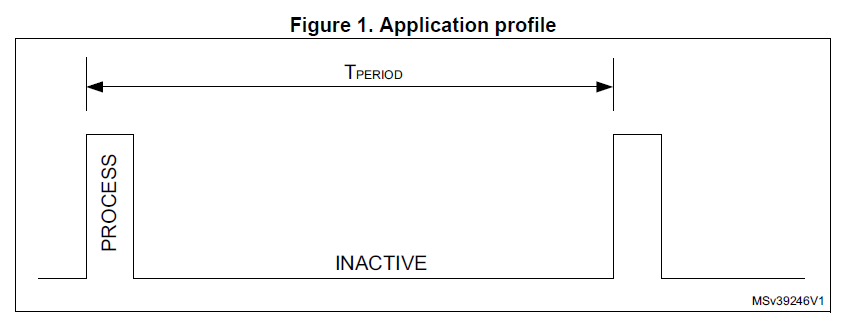
Buoy Frame

The frame of the buoy is decomposed into 3 main parts. These are:

Timing and sequencing, Power Configuration, State Machine. The focus on development optimizing for power consumption as well as accuracy. The system requirements are extremely flexible since the required sampling rate is very slow For example, the largest consideration of the system is Accelerometer sensing which has a maximum expected sample rate of 100Hz. For this reason, high speed computing techniques are not required and do not require much optimization. Since the system will most likely be in a wait state for the majority of its operation, It is important to place the device in as low power mode as possible to minimize consumption. This will be elaborated on in the following sections

The biggest Consideration with system operation is clock speed and source. The STM32l4 has 5 possible options: 3 internal oscillators (MSI,LSI,HSI) and 2 external crystal oscillators (HSE and LSE) these clock sources will provide power to the peripherals as well as the RTC. According the reference manual, the real time clock must be clocked from the LSE 32.768KHz crystal in order to provide an accurate calendar function therefore, the RTC must be clocked from the LSE no exceptions. The external crystal oscillators provide high precision clock speed with extremely low drift however, the power consumption of these oscillators are much higher than the internal RC. The clock configuration of the STM32L4 allows for a combination of these oscilators in a PHASE LOCKED LOOP (PLL) which allows for a greater degree of accuracy at desired speeds. The following information comes from Application note AN4746: Optimizing power with performance

Ultra Low power operations are described as applications with long periods of waiting followed by very short periods of processing

The Figure above details a typical low power operation Which can be expected from the buoy For a typical application, we consider two main phase:

1. Process phase: where peripherals need to be processed at regular intervals
2. Inactive phase: where system is asleep until RTC/GPIO event

Note: for the buoy, we consider two forms of inactivity: case 1: the buoy is inactive between samples. Consider the fact that the buoy is designed to operate in routines occurring once every half an hour. Once the routine is complete, it still has to wait an extroadinary long time before it is required again. This is the inactive between sample mode and consider this our period of inactivity where we can place the device in the **lowest possible state with very little concern for wake-up time or peripheral settings.**

Case 2: The buoy is inactive between data samples. As mentioned before, the buoy communicates with devices at relatively low sample rates: in the range of milliseconds to seconds. Add to that DMA transfers and the system has a significant amount of wait time. Therefore, we need to place the device in **low power mode however, it is crucial to maintain register configurations as well as provide a sufficient wake up/ response time.**

Therefore, we have 3 modes we need to optimize for:

1. Processing
2. Inactive between samples
3. Standby for data

In terms of wake up, the application note outlines the following transitions:

1. Sleep-to-run: Requires fast wake up with small in rush current
2. Run-to-sleep: flexible wake up with smallest energy consumption

The performance of the device can be evaluated using the ULP benchmark (section 1.2 )

# STM32L4 Power Modes

All the power modes (excluding shutdown) allow for the use of Brown out reset safeguards and IWDG.

The stm32l4 has 7 low power modes each with different effects in the microcontroller.

To reduce power consumption the following can be put in place.

1. Core logic can be supplied by low-power-voltage regulator to reduced quiescent current
2. The flash memory can be switched off in low power sleep mode
3. Flash memory can be switched off in low power run mode where program is loaded into SRAM
4. System Clock can be limited to 2MHz max using MSI controller

In addition, batch acquisition mode allows for data to be transferred with communication peripherals while the device is in low power mode

This can be achieved with the following configurations

1. Only DMA, Communication peripherals and SRAM1, SRAM2 clocks are enabled
2. Flash Memory is off
3. System clock is limited to 2 MHz

This allows for I2C and USART/LPUSART to be used in BATCH acquisition mode with the HSI oscillator therefore, this mode is suitable for use with GPS and IMU

The stm32l4 has 3 stop modes with full SRAM and Peripheral retention capabilities/capacity to wake up in 1 us with MSI up to 48MHz

In this mode, HSE,MSI,HIS are stopped while low speed oscillators are kept active. Peripherals can be set active using HIS clock when needed to wake up the device on some specific events ie I2c/ USART character recognition.

Standby Mode:

On the stm32l476RG, the device retains 32kB of SRAM2 at 230nA of current. BOR is always enabled.

Shutdown mode:

Shut down mode consumes the lowest current of any mode: 8nA at 1.8V

All internal voltage regulators are switched off and external power monitoring pin is disabled. Wake up from this mode can be done using one of 5 wake up pins or the reset pin. The RTC stays on provided it is clocked by the LSE

# Run Mode Power Consumption

The device was benchmarked by running a Fibonacci number sequence at 3.0V

A close up of text on a white background

Description automatically generated

Note: the highest power consumption is at clock speed 80MHz in Run range 1. Ideally, for current consumption: the clock speed should be between 100KHz and 26 MHz

A close up of a map

Description automatically generated

Note: the Highest Power efficiency is obtained in Run range 2, @ 26MHz

**Therefore: Active run mode will be run range 2, 26MHz**

# Low Power Mode Selection

Assuming a constant set of instructions with an application waking up every Tperiod to perform a function with Time: Tprocess

Tinactive = Tperiod-Tprocess

Lets assume that Tperiod >> Tprocess Thus we can simplify

Tinactive = Tperiod

The current over the period Iavg = Iprocess \* Tprocess/Tperiod + Iinactive\*(Tperiod-Tprocess)/Tperiod

The following modes are considered for inactive phase:

Assuming 24 MHz clock speed from MSI in PLL with LSE @32.768KHz and ambient Temperature of 25 C.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Mode** | **Features** | **Wake Up Time** | **Current Consumption @100 cps** | **Current consumption @1000000 cps** |
| Sleep/LP Sleep | Highest Reactivity. main regulator is off and the low power regulator (LPR) supplies low power to the VCORE domain, preserving the  contents of the registers, SRAM1 and SRAM2. | 6 clock cycles | 20 uA | 150 uA |
| Stop 0 | Wakeup timing critical. Both regulators turned on, main regulator supplies uC | < 1uS (if code in SRAM) | - |  |
| Stop 1 | When lots of peripherals need to stay awake and system has multiple sources of wake up. main regulator is off and the low-power regulator (LPR) supplies low power to the VCORE domain, preserving the contents of the registers, SRAM1 and SRAM2. | 6.3 uS from Flash Memory | 6uA | 120uA |
| Stop 2 | Few Peripherals Required, can generate wake up events ie LPUART reception LPTIM/ I2C Slave Address recognition main regulator is off and the low-power regulator (LPR) supplies low power to the VCORE domain, preserving the contents of the registers, SRAM1 and SRAM2. | 8.2 us from flash memory | 1.8uA | 110uA |
| Standby | No other peripherals than RTC need to stay awake and 32KB data retention required | 14 us from Flash Memory | 900 nA | 110uA |
| Shutdown | Only RTC and backup registers required to stay awake. th regulators are powered off. When exiting from Shutdown  mode, a power-on reset is generated | 256 us | 600nA | 110uA |

Note: consumption deltas become insignificant for processing cycles > 100,000. Shutdown mdoe has no data retention whatsoever thereby producing the lowest current consumption

Since, the device will be inactive for long periods of time with virtually no processing, the device will be placed into shutdown mode when device is inactive.

# Impact of Transitions

The Stm32L4 requires very low current to reload its internal nodes. The following is a table showing the energy consumption each transition takes at Vdd = 3.00V

|  |  |
| --- | --- |
| Transition | Energy consumption |
| Stop 1 to Run range 2 | 32nJ |
| Stop 2 to Run Range 2 | 50nJ |
| Standby to Run Mode 1 (MSI 4MHz) | 100nJ |
| Shutdown to Run Mode 1 | 460nJ |

According to Tables 2 and 3, the impact of wake up energy has a significant effect on the overall current consumption. The lowest possible current consumption of Stop2 and standby mode is achieved when cycles per second = 1000 and Tperiod = 10s (1 uA for standby and 1.78 uA for Stop 2), conversely, the highest possible current achieved for a 1ms period and 10,000,000 cps is (1163 and 1146 uA for standby and Stop 2 respectively) it should be noted that for the buoy the Tperiod will be orders of magnitude larger than 10s and therefore can result in even less current. Stop 2 mode is advisable for wake up periods < 20ms in 25 C temperatures provided the CPS is very high. Note that in Figure 8, Chapter 3.6, in a comparison between standby mode and shut down mode, Shut down mode will consume 20% less power than standby mode for Tperiod > 10s. IT should also be noted that as the cps increases, this difference becomes less and less significant. If cycles per second > 1M, there is virtually no difference between the two.

Note: a correction factor is required to apply for run range 2 for varying voltages and temperature. At High temps, this correction factor is > 1 and increases as Vdd Increases. For Temp = 25C the correction factor is 1 when Vdd is 3.00V. This is true for all power modes too. See figure 10. Additionally, for temps above 45 degrees, the the low power mode consumption doubles every 17 degrees. Over the whole temperature range, the same is true. The note also claims that in inactive mode, reducing the voltage from 3V to 1.8V reduces the current consumption by 12%

# Conclusion

In conclusion the following decision has been made regarding the Power modes of the device

|  |  |
| --- | --- |
| **Operation** | **Power Mode Choice** |
| Processing | Run Mode 2 |
| Inactive between Samples | Shutdown |
| Inactive between Data | Stop Mode 2 |

Note that these modes define behavior for the main loop. Should asynchronous behavior be introduced, additional consideration will be required to asses the required power mode. In addition, The application note makes no mention of low temperature optimization. Additional research will have to be done into run time.

Finally, a decision has been made to standardize the clock configuration as follows

|  |  |
| --- | --- |
| Run mode System Clock source: | MSI + LSE PLL |
| Clock Frequency: | 24MHz |
| Shut down mode clock source | LSE |
| RTC Clock frequency | 1Hz |
| LSE clock frequency | 32.768 KHz |
| Standby for data clock source: |  |

# Power Reset

The Device has an integrated power on reset, Power Down Reset and Brown Out Reset. This mode is active in all power modes except Shut down mode and cannot be disabled. 5 thresholds can be set for brown out reset. During power on, BOR keeps the device under reset until enough voltage is reached.

# Transition Map

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Mode | Run | Sleep | LP Run | LP Sleep | Stop 0 | Stop 1 | Stop 2 | Standby | Shut down |
| Run | - | Y | Y | N | Y | Y | Y | Y | Y |
| Sleep | Y | - | N | N | N | N | N | N | N |
| LP Run | Y | N | - | Y | N | Y | N | Y | Y |
| LP Sleep | N | N | Y | - | N | N | N | N | N |
| Stop 0 | Y | N | N | N | - | N | N | N | N |
| Stop 1 | Y | N | Y | N | N | - | N | N | N |
| Stop 2 | Y | N | N | N | N | N | - | N | N |
| Standby | Y | N | N | N | N | N | N | - | N |
| Shutdown | Y | N | N | N | N | N | N | N | - |

From Sleep and stop mode, the MCU exits low power mode depending on the way that the low power mode was entered. If the WFI instruction/ return from interrupt was used, then any nvic event can wake system up. If the WFE instruction was used, the MCU exits the low power mode as soon as an event occurs.

From Standby mode and shutdown mode, the MCU exits low power mode through an external reset, IWDG reset, rising edge on wakeup pin or RTC event. Program effectively starts again.

# Stop Mode 2

|  |  |
| --- | --- |
| Entry Condition | Program is waiting for data from a sensor/ used with peripherals that require long waits between data ie GPS, Iridium and IMU |
| Entry | Set WFI bit  Set DEEPSLEEP bit in Cortex-M4 System Control Register  No Interrupts/ Events are pending  LPMS = 001 in PWR control |
| Exit | Any EXTI Line configured in Interrupt Mode  -GPS – UART4  -Iridium – UART5  -I2c – I2c1 |

# Shut down Mode